



# P24C08D/P24C16D

## I<sup>2</sup>C-Compatible Serial E<sup>2</sup>PROM

### Datasheet V1.5

### General Description

The P24C08D/P24C16D is I<sup>2</sup>C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 8 Kbits (1 Kbytes)/16 Kbits (2 Kbytes), which is 16 bytes per page.

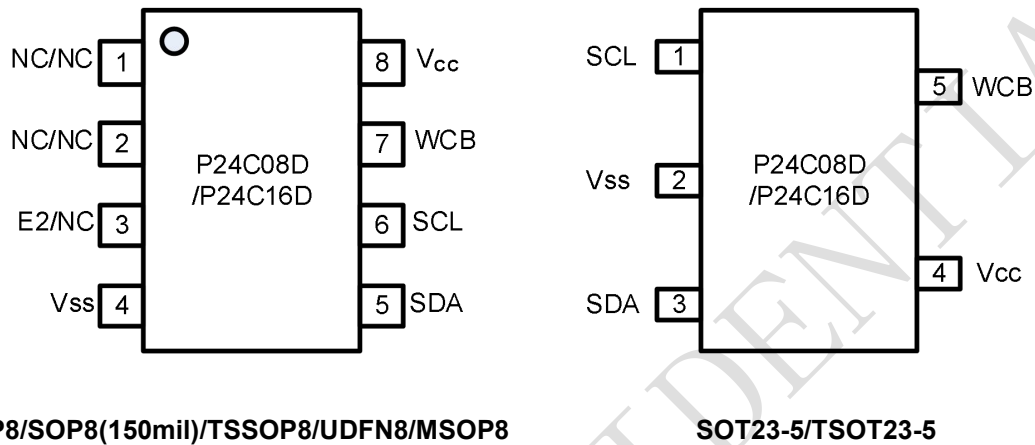
### Features

- Single Supply Voltage and High Speed Mode
  - ◇ Minimum operating voltage down to 1.7 V
  - ◇ 400 kHz/1 MHz clock from 1.7V to 5.5 V
- Low power CMOS technology
  - ◇ Read current 0.2 mA (400 kHz, typical)
  - ◇ Write current 0.8 mA (400 kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Page and 128 bits Serial Number
- Self-timed Write Cycle (5 ms maximum)
- High Reliability
  - ◇ Endurance: 1 Million Write Cycles
  - ◇ Data Retention: 100 Years
  - ◇ HBM: 4 kV
  - ◇ Latch up Capability: +/-200 mA(25 C)
- Package: PDIP8, SOP8(150mil), TSSOP8, SOT23-5, TSOT23-5, UDFN8, MSOP8

## 1. Pin Configuration

### 1.1 Pin Configuration

Figure 1-1 Pin Configuration



PDIP8/SOP8(150mil)/TSSOP8/UDFN8/MSOP8

SOT23-5/TSOT23-5

### 1.2 Pin Definition

Table 1-1 Pin Definition for PDIP8/SOP8(150mil)/TSSOP8/UDFN8/MSOP8 Packages

Pin	Name	Type	Description
1	NC	\	No Connect
2	NC	\	No Connect
3	E2	Input	Slave Address Setting (only for P24C08D)
4	Vss	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	Vcc	Power	Power

Table 1-2 Pin Definition for SOT23-5/TSOT23-5 Packages

Pin	Name	Type	Description
1	SCL	Input	Serial Clock Input
2	Vss	Ground	Ground
3	SDA	I/O	Serial Data Input and Serial Data Output
4	Vcc	Power	Power
5	WCB	Input	Write Control, Low Enable Write

### 1.3 Pin Descriptions

**Serial Clock (SCL):** The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

**Serial Data (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

**Write Control (WCB):** The Write Control input, when WCB is connected directly to  $V_{CC}$ , all write operations to the memory are inhibited. When connected to  $V_{SS}$ , allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to  $V_{SS}$ .

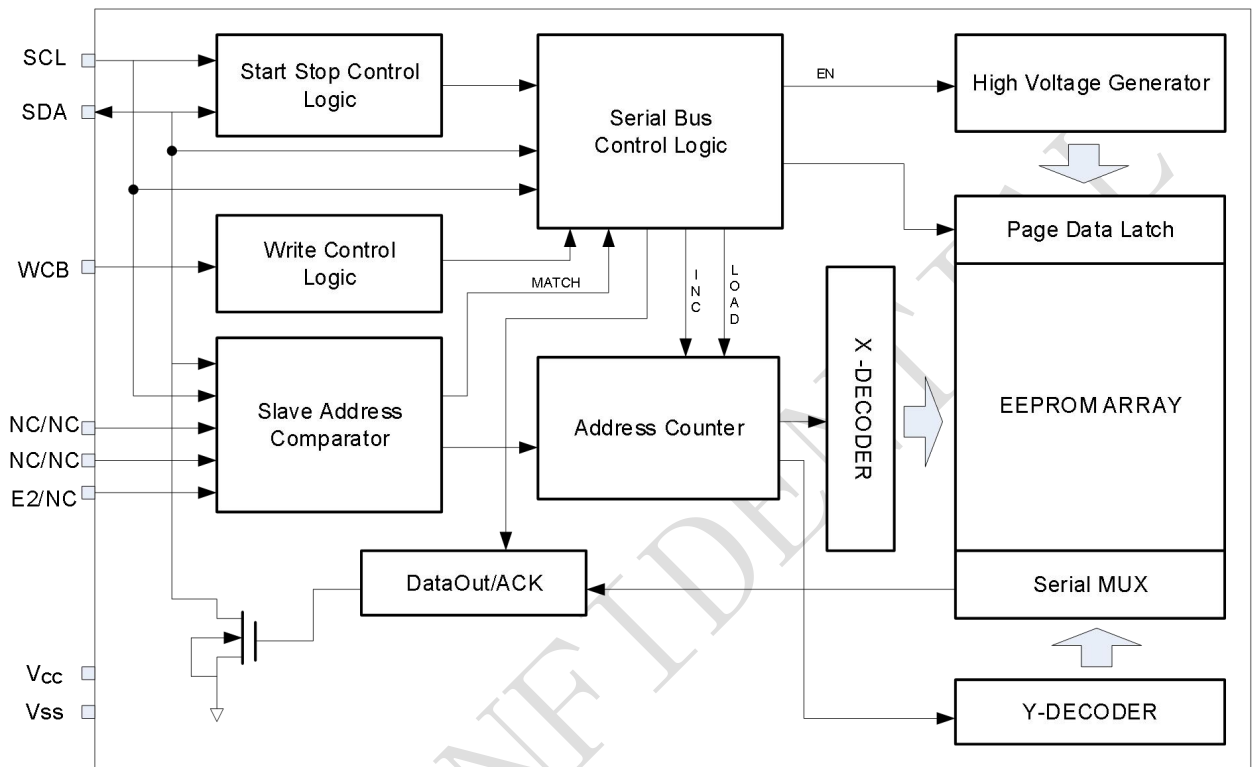
**Device Addresses (E2):** The E2 pin is device address inputs. Typically, the E2 pin is for hardware addressing and a total of 2 devices can be connected on a single bus system. If these pins are left floating, the E2 pin will be internally pulled down to  $V_{SS}$ , and the corresponding device address is fixed to 0.

**Supply Voltage( $V_{CC}$ ):**  $V_{CC}$  is the supply voltage.

**Ground( $V_{SS}$ ):**  $V_{SS}$  is the reference for the  $V_{CC}$  supply voltage.

## 2. Block Diagram

Figure 2-1 Block Diagram



### 3. Electrical Characteristics

**Table 3-1 Absolute Maximum Ratings** <sup>[1]</sup>

Symbol	Parameter	Min.	Max.	Units
T <sub>STG</sub>	Storage Temperature	-65	150	°C
T <sub>A</sub>	Ambient operating temperature	-40	85	°C
V <sub>CC</sub>	Supply Voltage	-0.5	6.5	V
V <sub>IO</sub>	Input or output range	-0.5	6.5	V
I <sub>OL</sub>	DC output current (SDA=0)	-	5	mA

Note: [1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 3-2 Pin Capacitance** <sup>[1]</sup>

Symbol	Parameter	Max.	Units	Test Condition
C <sub>I/O</sub>	Input / Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = V <sub>SS</sub>
C <sub>IN</sub>	Input Capacitance (WCB, SCL)	6	pF	V <sub>IN</sub> = V <sub>SS</sub>

Note: [1] Test Conditions: T<sub>A</sub> = 25°C, f<sub>SCL</sub> = 1MHz, V<sub>CC</sub> = 5.0V.

**Table 3-3 DC Characteristics** (Unless otherwise specified, V<sub>CC</sub> = 1.7V to 5.5V, T<sub>A</sub> = -40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V <sub>CC</sub>	Supply Voltage	1.7	-	5.5	V	
		1.8	-	5.5	V	
		2.5	-	5.5	V	
I <sub>sb</sub>	Standby Current (Standby mode)	-	0.5	1.0	uA	V <sub>CC</sub> = 1.7V
		-	0.8	2.0	uA	V <sub>CC</sub> = 3.3V
		-	1.0	4.0	uA	V <sub>CC</sub> = 5.5V
I <sub>CC1</sub>	Supply Current (Read)	-	0.2	0.4	mA	V <sub>CC</sub> = 5.5V, f <sub>SCL</sub> = 400 KHz
I <sub>CC2</sub>	Supply Current (Write)	-	0.8	1.6	mA	V <sub>CC</sub> = 5.5V, f <sub>SCL</sub> = 400 KHz
I <sub>LI</sub>	Input Leakage Current	-	0.10	1.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>
I <sub>LO</sub>	Output Leakage Current	-	0.05	1.0	μA	V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub>
V <sub>IL</sub>	Input Low Level	-0.5	-	0.3V <sub>CC</sub>	V	
V <sub>IH</sub>	Input High Level	0.7V <sub>CC</sub>	-	V <sub>CC</sub> +0.5	V	
V <sub>OL1</sub>	Output Low Level V <sub>CC</sub> = 1.7V (SDA)	-	-	0.2	V	I <sub>OL</sub> = 0.15 mA
V <sub>OL2</sub>	Output Low Level V <sub>CC</sub> = 3.0V (SDA)	-	-	0.4	V	I <sub>OL</sub> = 2.1 mA

**Table 3-4 400kHz&1MHz AC Characteristics** ( Unless otherwise specified,  $V_{CC} = 1.7V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ ,  $C_L=100pF$ , Test Conditions are listed in Notes [2] )

Symbol	Parameter	1.7≤V <sub>CC</sub> ≤5.5			1.7≤V <sub>CC</sub> ≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f <sub>SCL</sub>	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t <sub>LOW</sub>	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t <sub>HIGH</sub>	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t <sub>AA</sub>	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t <sub>I</sub>	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t <sub>BUF</sub>	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
t <sub>HD.STA</sub>	Start Hold Time	0.6	-	-	0.25	-	-	μs
t <sub>SU.STA</sub>	Start Setup Time	0.6	-	-	0.25	-	-	μs
t <sub>HD.DAT</sub>	Data In Hold Time	0	-	-	0	-	-	μs
t <sub>SU.DAT</sub>	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t <sub>R</sub>	Inputs Rise Time <sup>[1]</sup>	-	-	0.3	-	-	0.3	μs
t <sub>F</sub>	Inputs Fall Time <sup>[1]</sup>	-	-	0.3	-	-	0.1	μs
t <sub>SU.STO</sub>	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t <sub>DH</sub>	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
t <sub>SU.WCB</sub>	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
t <sub>HD.WCB</sub>	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t <sub>WR</sub>	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- ✧ R<sub>L</sub> (connects to V<sub>CC</sub>): 1.3k (2.5V, 5.5V), 10k (1.7V)
- ✧ Input pulse voltages: 0.3 V<sub>CC</sub> to 0.7 V<sub>CC</sub>
- ✧ Input rise and fall times: ≤50ns
- ✧ Input and output timing reference voltages: 0.5V<sub>CC</sub>

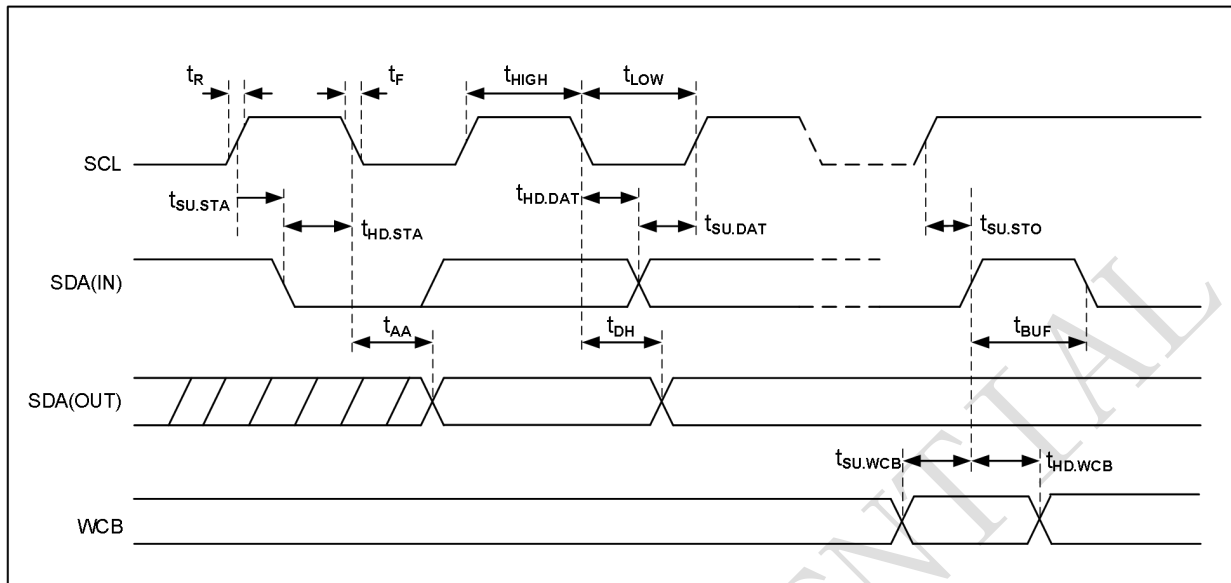
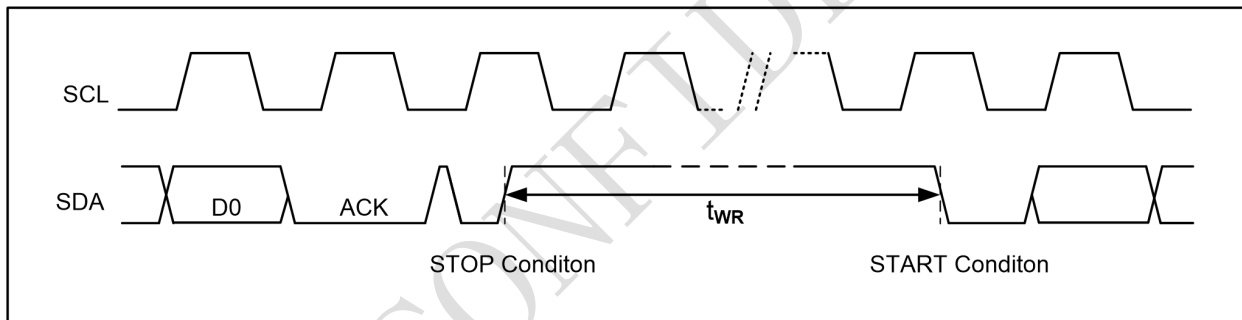
**Table 3-5 Reliability Characteristic** <sup>[1]</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR <sup>[2]</sup>	Endurance	1,000,000			Write cycles
DRET <sup>[3]</sup>	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

[3] Test condition: T<sub>A</sub> = 55°C

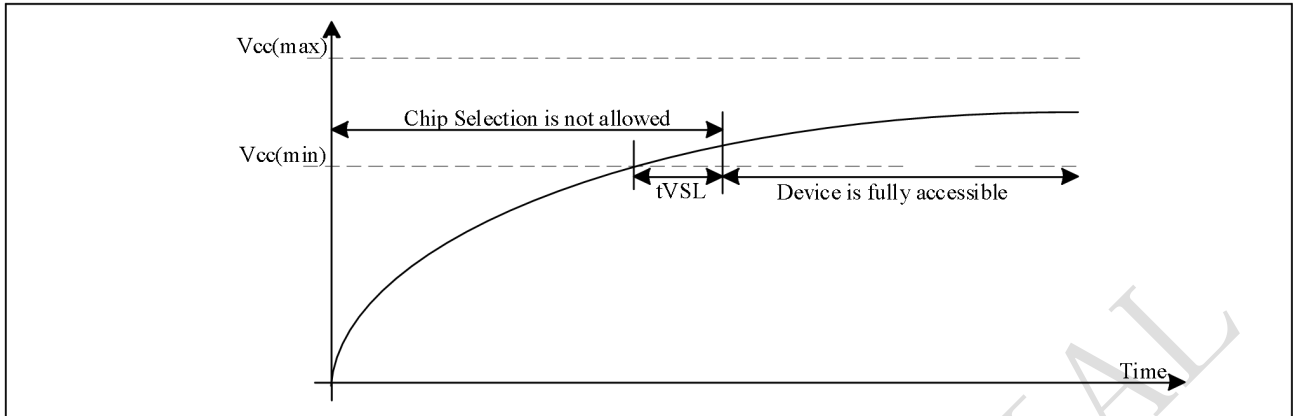
**Figure 3-1 Bus Timing****Figure 3-2 Write Cycle Timing**

Note: [1] The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

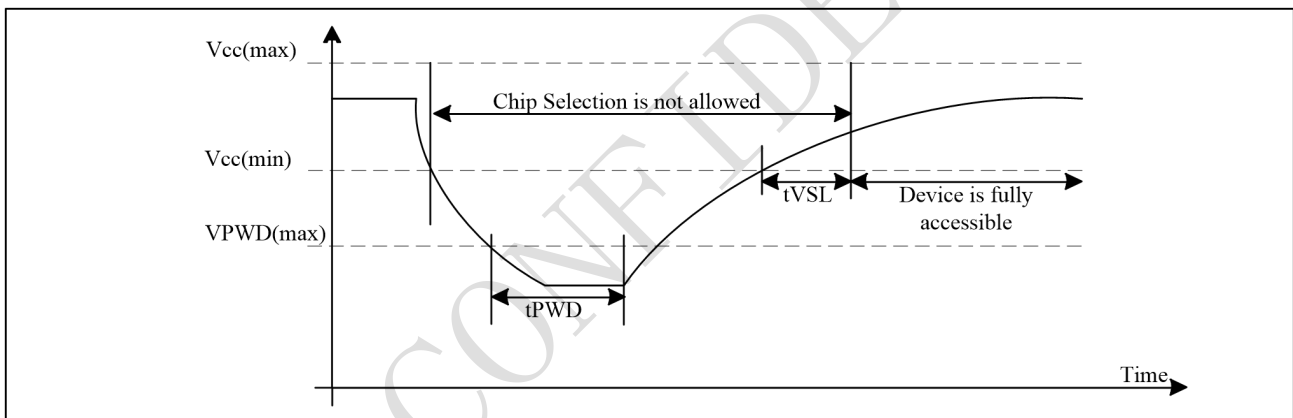
### Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status.  $t_{VSL}$  is the time required to initialize the EEPROM. No instructions are accepted during this time.

**Figure 3-3 Power up Timing****Power Up/Down and Voltage Drop**

For Power-down to Power-up operation, the VCC of EEPROM device must be below VPWD for at least tPWD timing. Please check the table below for more detail.

**Figure 3-4 Power down-up Timing**

Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	70		us
tVR	VCC Rise Time	1	500000	us/V

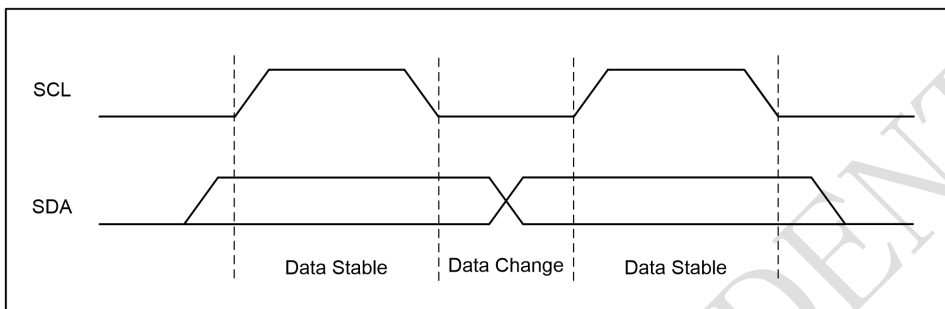


## 4. Device Operation

### 4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**Figure 4-1 Data Validity**



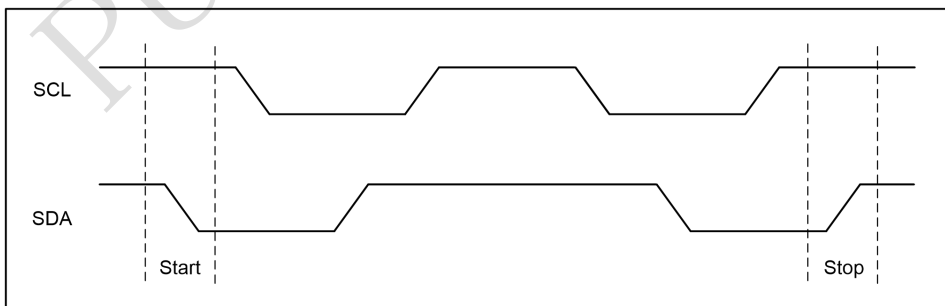
### 4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

### 4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the P24C08D/P24C16D in a standby mode (see Figure 4-2).

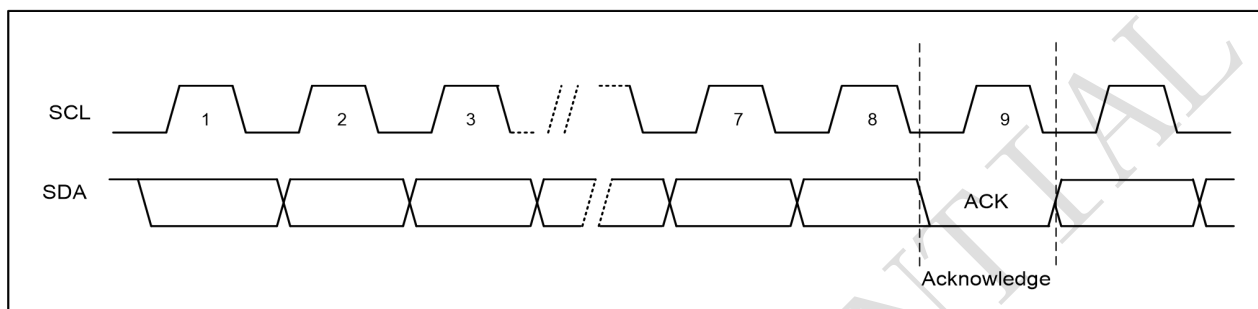
**Figure 4-2 Start and Stop Definition**



## 4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the P24C08D/P24C16D in 8-bit words. The P24C08D/P24C16D sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

**Figure 4-3 Output Acknowledge**



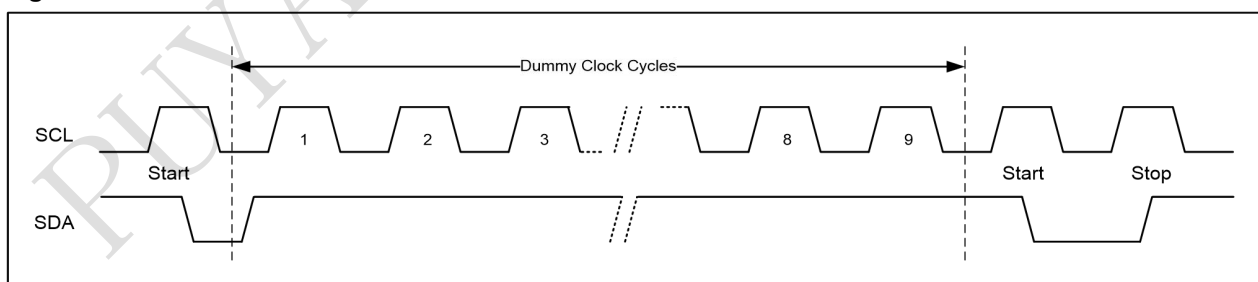
## 4.5 Standby Mode

The P24C08D/P24C16D features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

## 4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

**Figure 4-4 Soft Reset**



## 4.7 Device Addressing

The P24C08D/P24C16D requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

**Table 4-1 Device Address**

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C08D	Normal Area	1	0	1	0	E2	A9	A8	R/W
	ID Page	1	0	1	1	E2	X	X	R/W
	Lock Bit	1	0	1	1	E2	X	X	R/W
	Serial Number	1	0	1	1	E2	X	X	1
P24C16D	Normal Area	1	0	1	0	A10	A9	A8	R/W
	ID Page	1	0	1	1	X	X	X	R/W
	Lock Bit	1	0	1	1	X	X	X	R/W
	Serial Number	1	0	1	1	X	X	X	1

**Table 4-2 Word Address**

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C08D P24C16D	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	0	0	X	X	A3	A2	A1	A0
	Lock Bit	X	1	X	X	X	X	X	X
	Serial Number	1	0	X	X	A3	A2	A1	A0

The E2 device address bits to allow as many as two devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2 pin uses an internal proprietary circuit that biases it to a logic low condition if the pin is floating. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

## 4.8 Data Security

The P24C08D/P24C16D has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

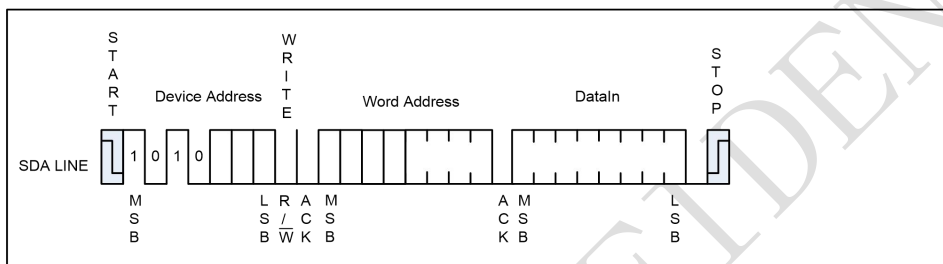
## 5. Instructions

### 5.1 Write Operations

#### 5.1.1 Byte Write

A write operation requires one 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the P24C08D/P24C16D will again respond with a “0” and then clock in the first 8-bit data. Following receipt of the 8-bit data word, the P24C08D/P24C16D will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the P24C08D/P24C16D enters an internally timed write cycle, all inputs are disabled during this write cycle and the P24C08D/P24C16D will not respond until the write is complete (see Figure 5-1).

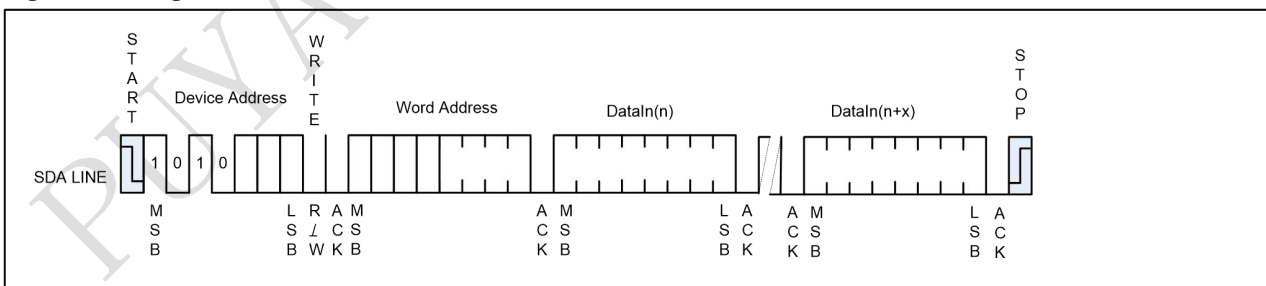
Figure 5-1 Byte Write



#### 5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the P24C08D/P24C16D acknowledges receipt of the first data word, the master can transmit more data words. The P24C08D/P24C16D will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the P24C08D/P24C16D, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

### 5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the P24C08D/P24C16D inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the P24C08D/P24C16D respond with a “0”, allowing the read or write sequence to continue.

### 5.1.4 Write Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Address bit A7~A6 must be ‘00’.
- Address bits A3~A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

### 5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A6 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

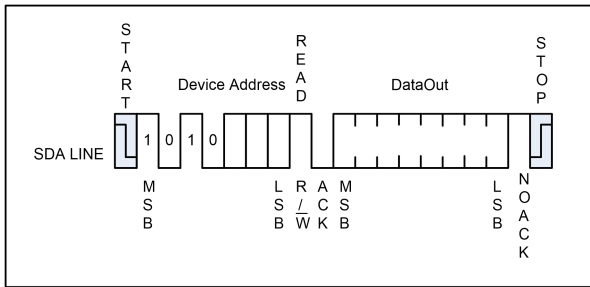
## 5.2 Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

### 5.2.1 Current Address Read

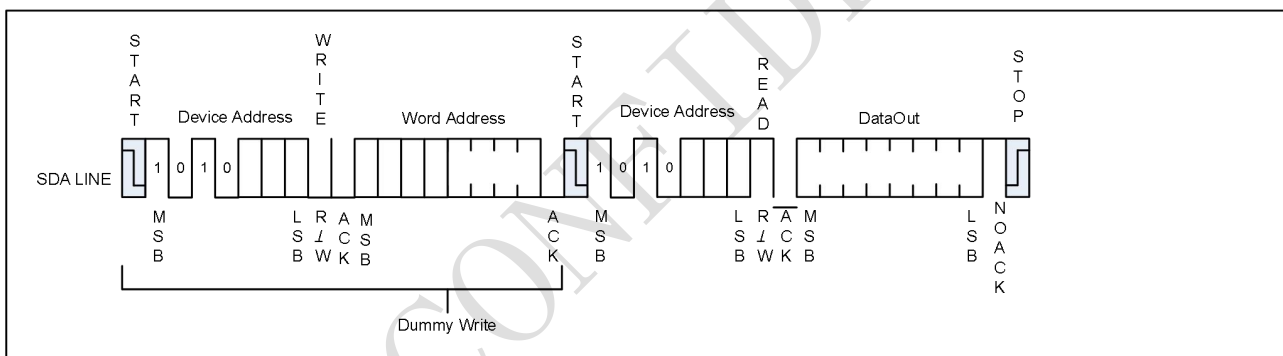
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the P24C08D/P24C16D, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 5-3).

**Figure 5-3 Current Address Read**

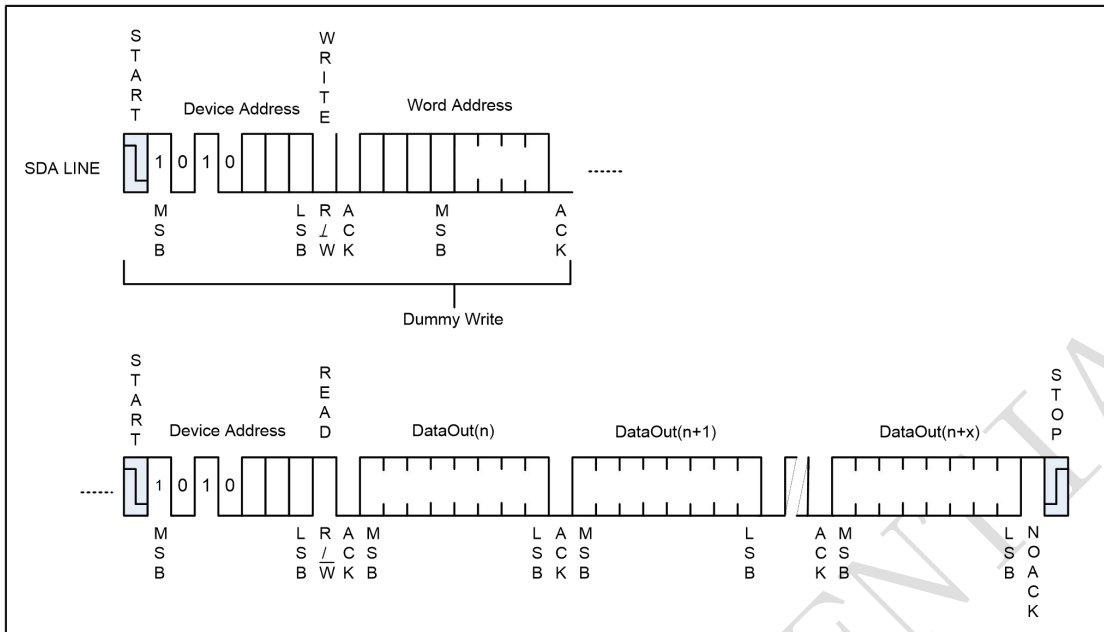
### 5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the P24C08D/P24C16D, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The P24C08D/P24C16D acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-4).

**Figure 5-4 Random Read**

### 5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the P24C08D/P24C16D receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-5)

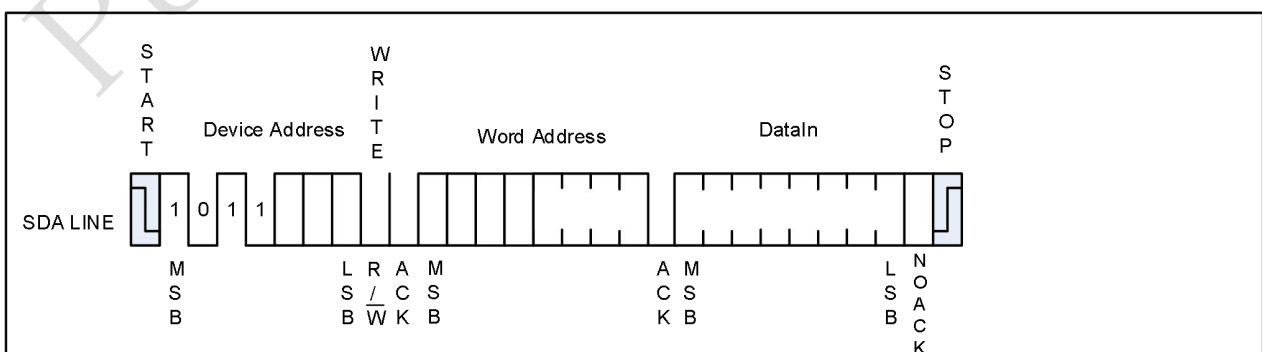
**Figure 5-5 Sequential Read**

#### 5.2.4 Read Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bit A7~A6 must be '00', and the LSB address bits A3~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 6, as the ID page boundary is 16 bytes).

#### 5.2.5 Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

**Figure 5-6 Lock Status Read (When Identification page locked, return NoACK after one data byte)**





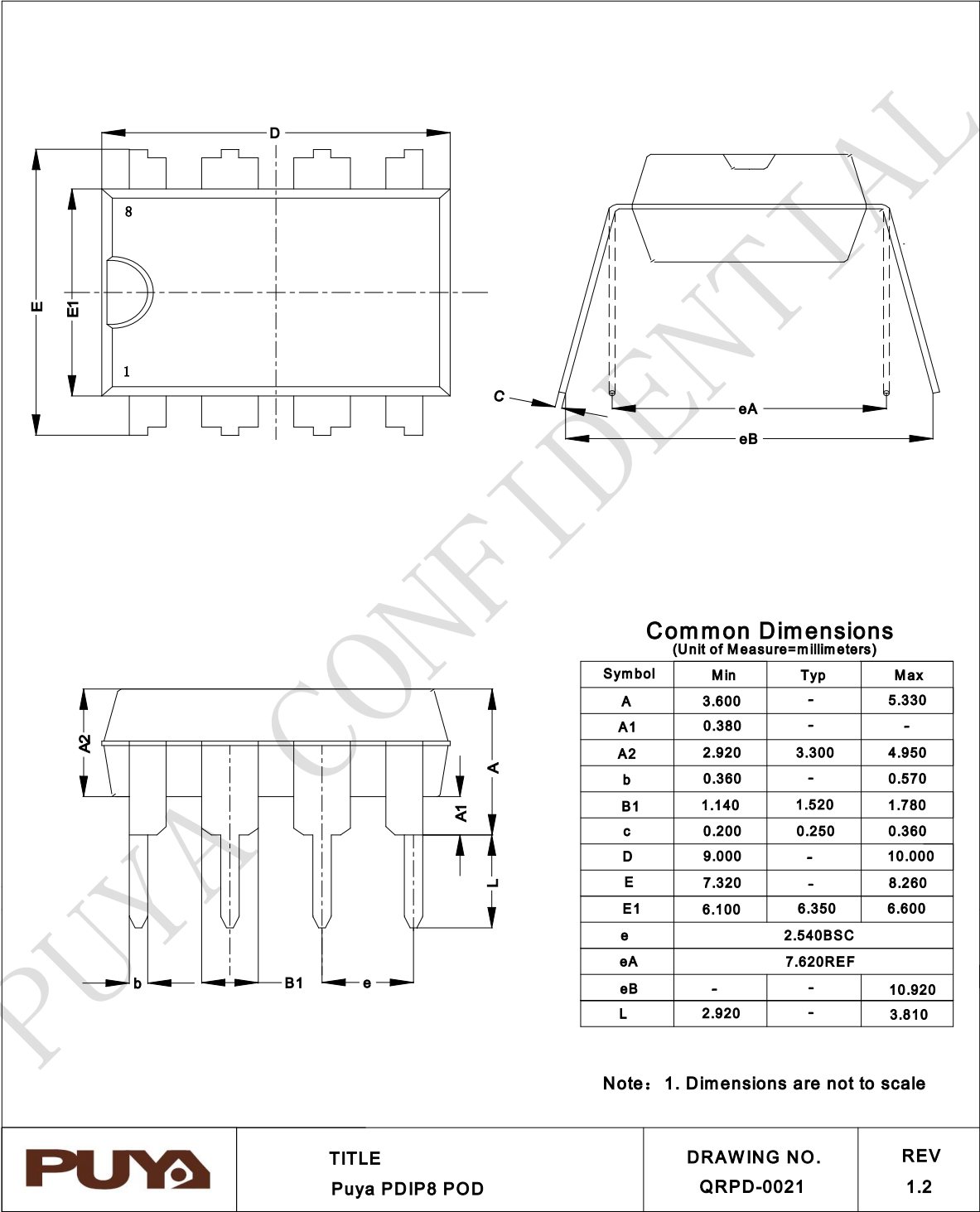
## 6. Ordering Code Detail

Example:

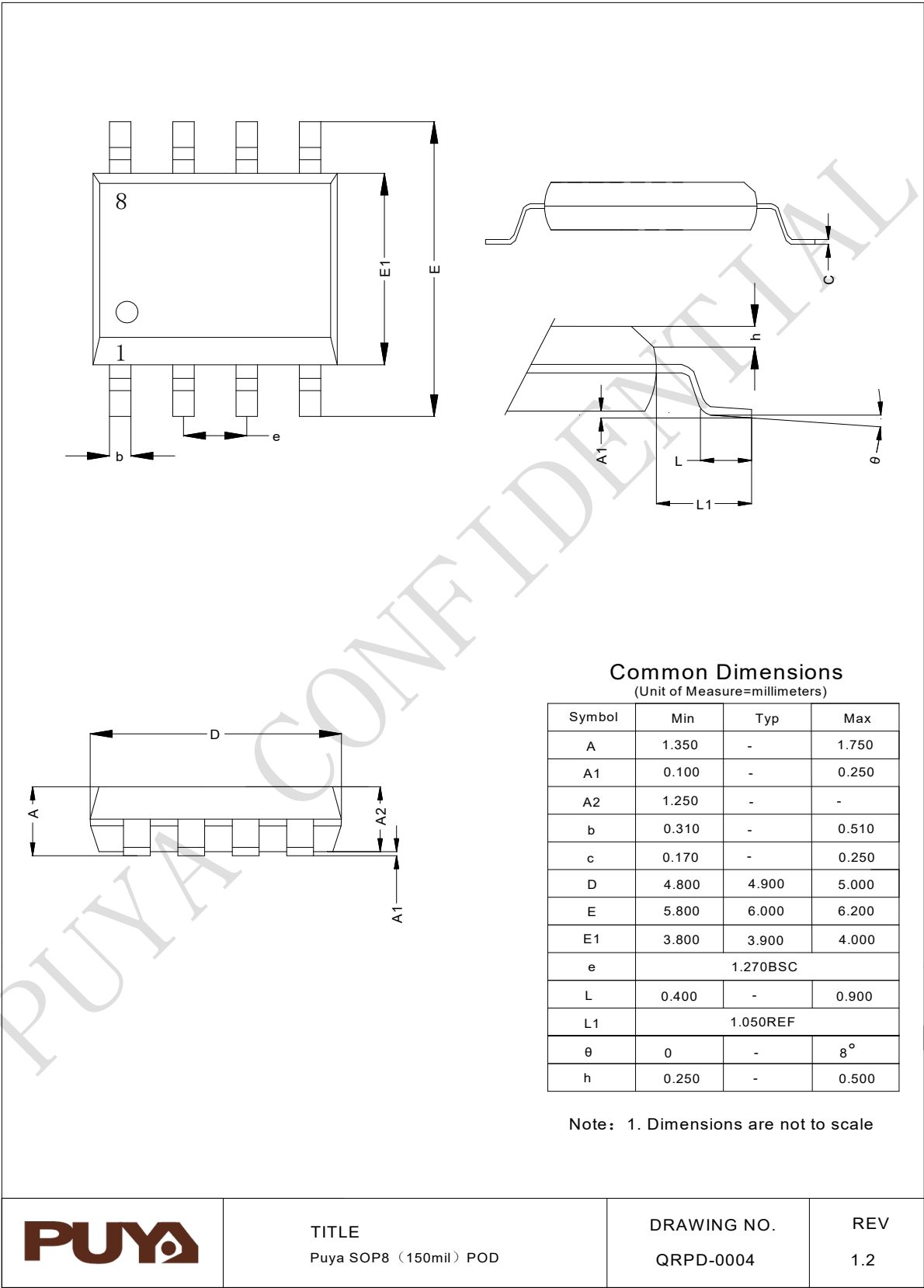
	P	2	4	C	16	D	-	S	S	H	-	M	I	R
<b>Company Designator</b>														
P = Puya Semiconductor														
<b>Product Series Name</b>														
24C = I2C-compatible Interface EEPROM														
<b>Device Density</b>														
08 = 8K bits														
16 = 16K bits														
<b>Device Version</b>														
D = Version D														
<b>Package Option</b>														
DP: PDIP8														
SS: SOP8(150mil)														
MS: MSOP8														
TS: TSSOP8														
UN: UDFN8														
WF: WAFER														
ST: SOT23-5														
TO: TSOT23-5														
<b>Plating Technology</b>														
H: RoHS Compliant, Halogen-free, Antimony-free														
<b>Operation Voltage</b>														
M: 1.7~5.5V														
N: 1.8~5.5V														
D: 2.5~5.5V														
<b>Device Grade</b>														
I: -40~85C														
<b>Shipping Carrier Option</b>														
W: WAFER														
T: TUBE														
R: TAPE & REEL														

7. Package information

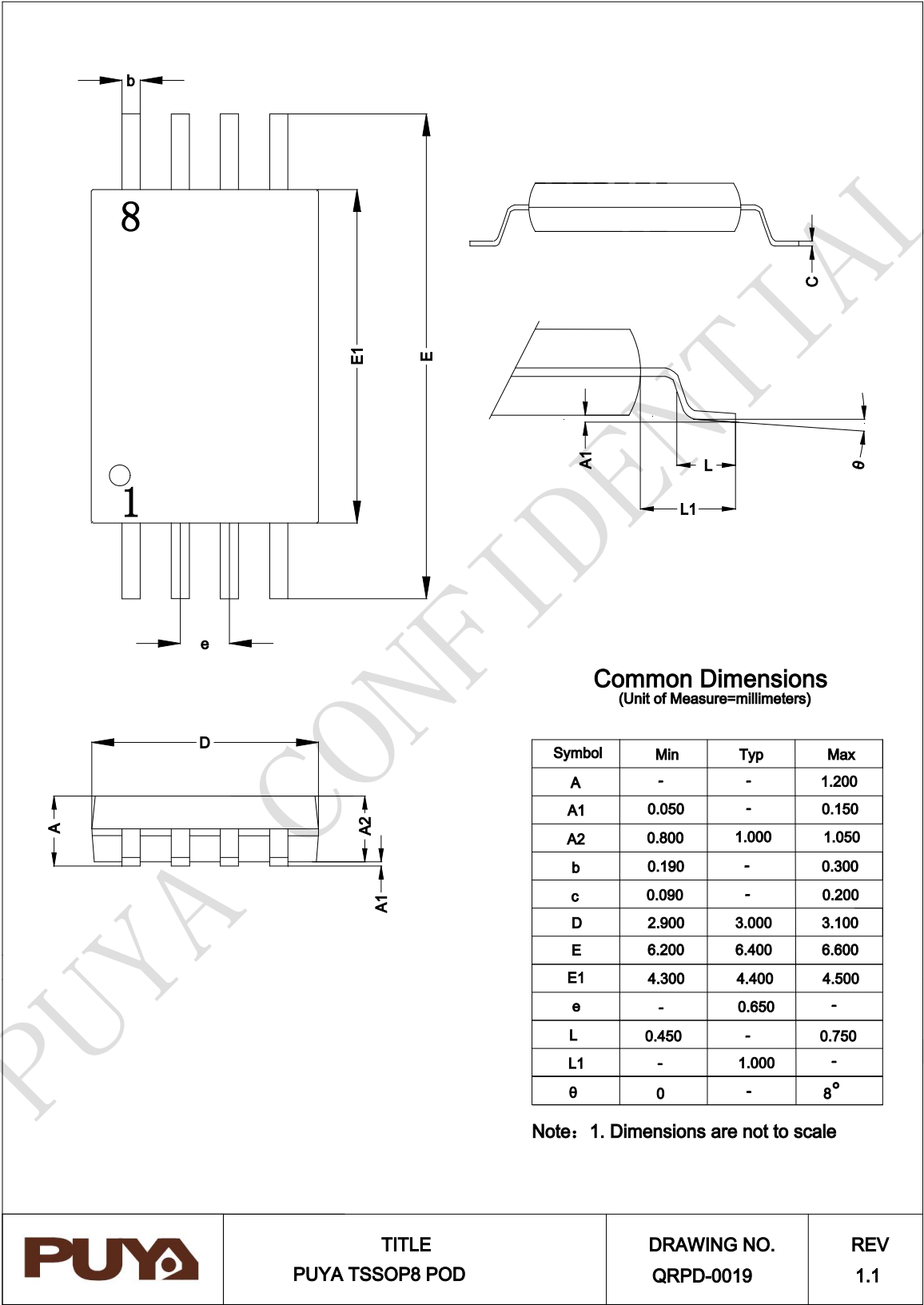
7.1 PDIP8



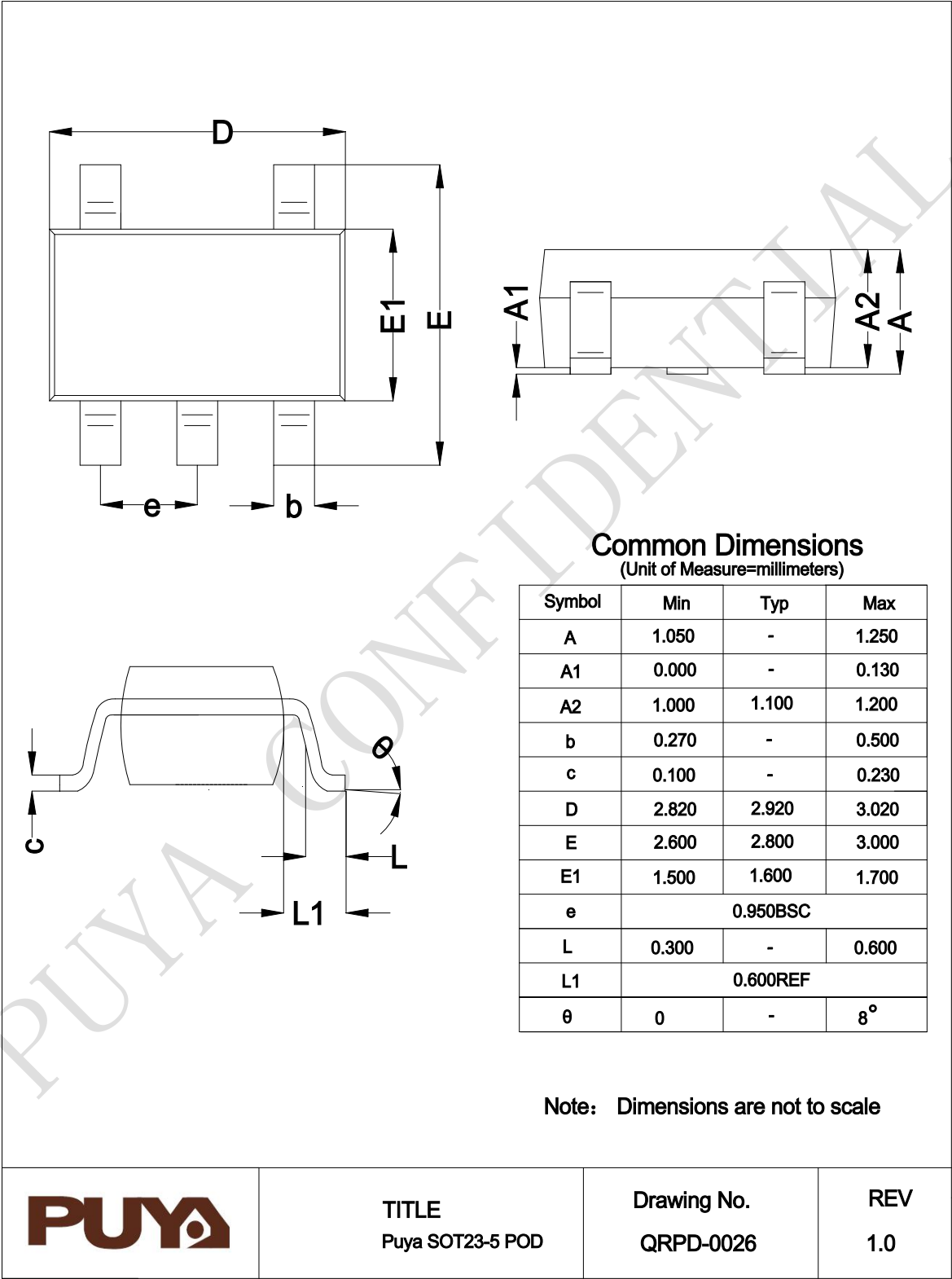
7.2 SOP8(150mil)



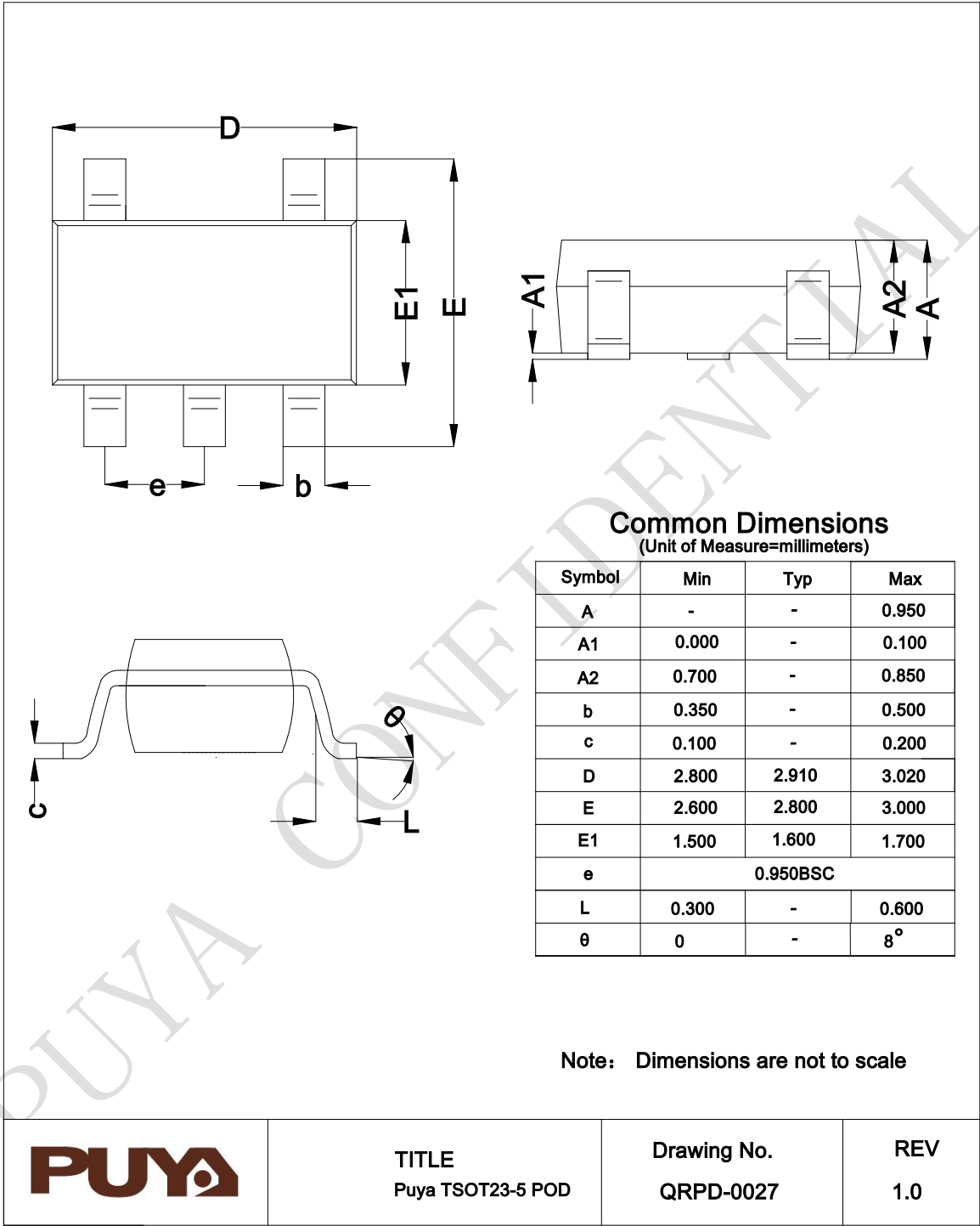
7.3 TSSOP8



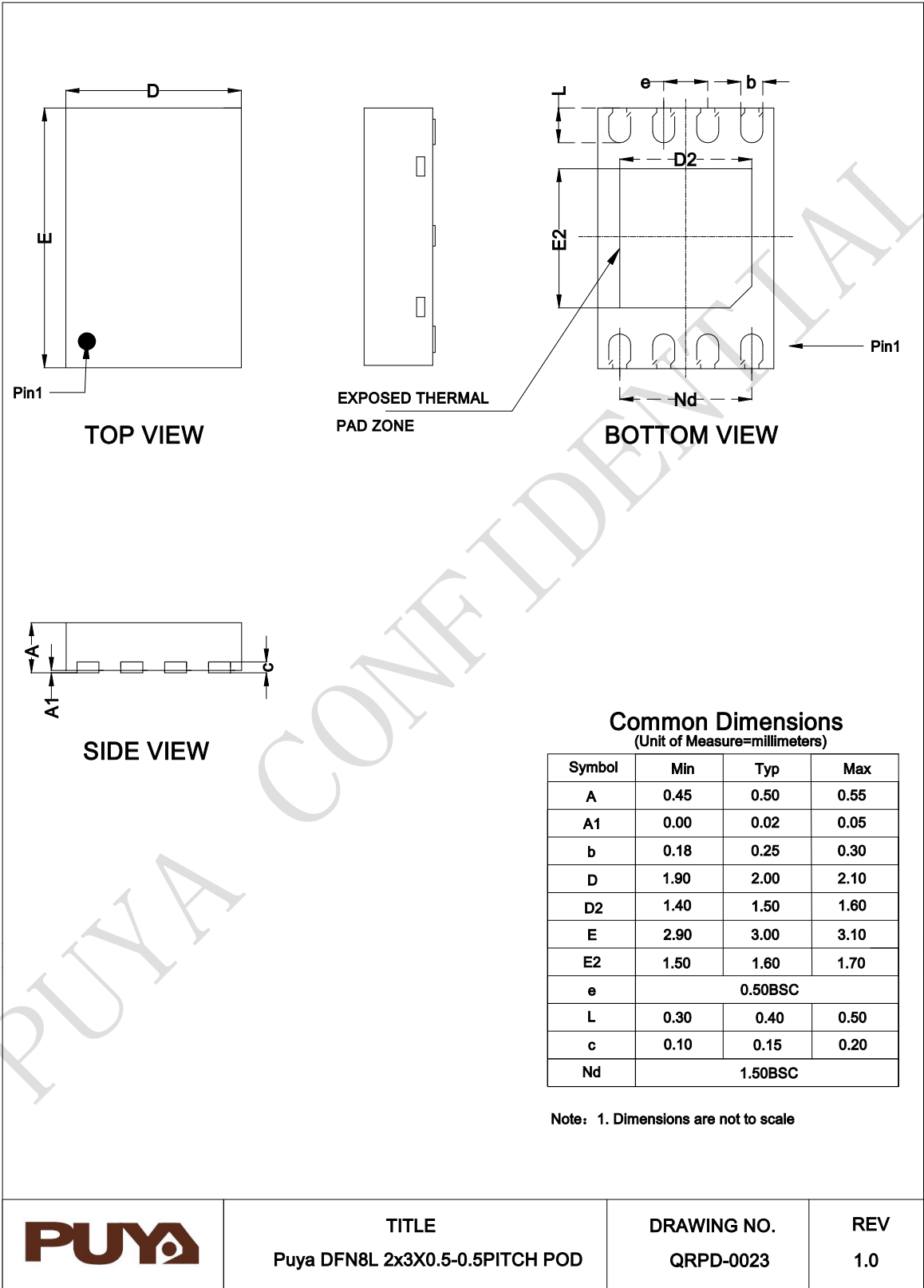
7.4 SOT23-5



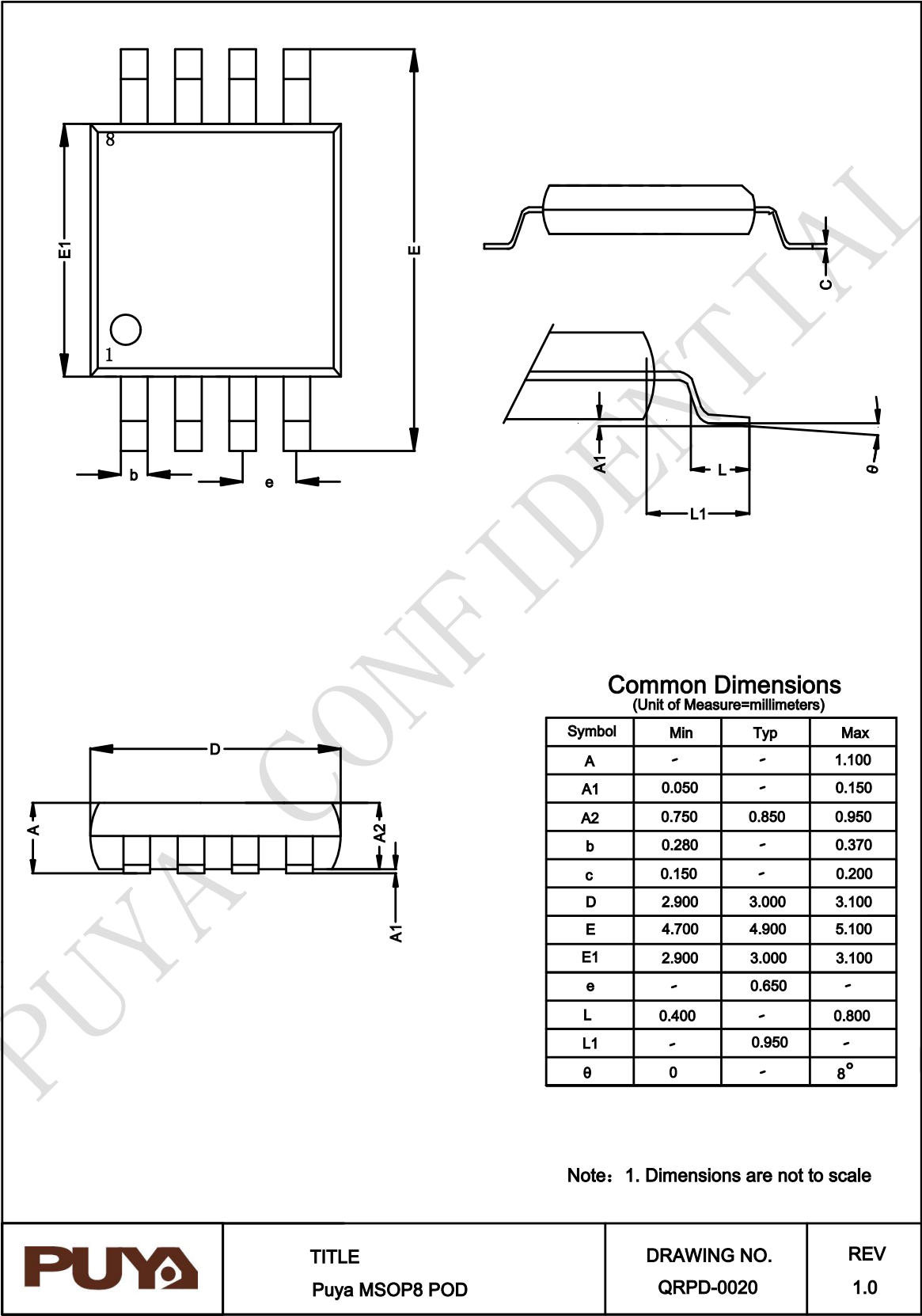
7.5 TSOT23-5



7.6 UDFN8



7.7 MSOP8





8. Revision History

Version	Content	Date
V1.0	Initial Release	2021-08-18
V1.1	Add Device Power up/Power down description	2022-03-10
V1.2	Update parameter of $V_{IL}$	2023-03-26
V1.3	Update figure of Package information	2024-02-20
V1.4	Update Table 4-1	2024-04-16
V1.5	(1) Update Features description (2) Update Pin Cofiguration (3) Update the $I_{sb}$ 、 $I_{CC1}$ and $I_{CC2}$ Description of 'Table 3-3 DC Characteristics' (4) Update Serial Number description (5) Update PDIP8 POD (6) Update SOP8(150mil) POD (7) Update SOT23-5 POD (8) Update TSOT23-5 POD	2025-06-16



Puya Semiconductor Co., Ltd.

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